L Number	Hits	Search Text	DB	Time stamp
1	174	PMOS and NMOS and (sidewalls same width)	USPAT; US-PGPUB	2002/10/29 10:05
2	81	(PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner))	USPAT; US-PGPUB	2002/10/29 10:07
3	58	((PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner))) and @ad<=20000518	USPAT; US-PGPUB	2002/10/29 10:06
4	2	PMOS and NMOS and (sidewalls same width)	EPO; JPO; DERWENT; IBM_TDB	2002/10/29 10:03
5	6	PMOS and NMOS and sidewalls and width	EPO; JPO; DERWENT; IBM_TDB	2002/10/29 10:04
6	16	CMOS and sidewalls and width	EPO; JPO; DERWENT; IBM_TDB	2002/10/29 10:04
7	15	(CMOS and sidewalls and width) not (PMOS and NMOS and sidewalls and width)	EPO; JPO; DERWENT; IBM_TDB	2002/10/29 10:04
8	551	CMOS and (sidewalls same width)	USPAT; US-PGPUB	2002/10/29 10:06
9	493	(CMOS and (sidewalls same width)) not ((PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner)))	USPAT; US-PGPUB	2002/10/29 10:06
10	443	(CMOS and (sidewalls same width)) and @ad<=20000518	USPAT; US-PGPUB	2002/10/29 10:07
11	400	((CMOS and (sidewalls same width)) and @ad<=20000518) not (((PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner))) and @ad<=20000518)	USPAT; US-PGPUB	2002/10/29 10:07
12	155	(((CMOS and (sidewalls same width)) and @ad<=20000518) not (((PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner))) and @ad<=20000518)) and (width same (different or larger or smaller or thicker or thinner))	USPAT; US-PGPUB	2002/10/29 10:20
13	218	(((CMOS and (sidewalls same width)) and @ad<=20000518) not (((PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner))) and @ad<=20000518)) and (width same (greater or less))	USPAT; US-PGPUB	2002/10/29 10:21
14	117	((((CMOS and (sidewalls same width)) and @ad<=20000518) not (((PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner))) and @ad<=20000518)) and (width same (greater or less))) not ((((CMOS and (sidewalls same width)) and @ad<=20000518) not (((PMOS and NMOS and (sidewalls same width)) and (width same (different or larger or smaller or thicker or thinner))) and @ad<=20000518)) and (width same (different or larger or smaller or thicker or thinner)))	USPAT; US-PGPUB	2002/10/29 10:21

US-PAT-NO: 5963803

DOCUMENT-IDENTIFIER: US 5963803 A

TITLE: Method of making N-channel and P-channel IGFETs with different gate thicknesses and spacer widths

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A method of making N-channel and P-channel IGFETs with **different** gate thicknesses and spacer widths is disclosed. The method includes providing a semiconductor substrate with a first active region of a first conductivity type and a second active region of a second conductivity type, forming a first gate over the first active region and a second gate over the second active region, wherein the second gate has a substantially greater thickness than the first gate, forming first spacers in close proximity to opposing **sidewalls** of the first gate and second spacers in close proximity to opposing **sidewalls** of the second gate, wherein the second spacers have a substantially greater **width** than the first spacers due to the second gate having a substantially greater thickness than the first gate, and forming a first source and a first drain of the second conductivity type in the first active region and a second source and a second drain of the first conductivity type in the second active region.

Preferably, the N-channel device is formed in the first active region, the P-channel device is formed in the second active region, and the N-channel and P-channel devices include lightly and heavily doped source and drain regions.

In this manner, the relatively thick gate for the P-channel

device reduces
boron penetration, and the relatively wide spacers for the P-channel device
offset the rapid diffusion of boron in the heavily doped source and drain
regions of the P-channel device during high temperature processing so that the
lightly doped source and drain regions for the N-channel and P-channel devices
have the desired sizes.

Complementary metal-oxide semiconductor (**CMOS**) circuits include N-channel and
P-channel devices. During **CMOS** manufacturing, the gates for the N-channel and
P-channel devices are typically formed by depositing a blanket layer of
polysilicon over the substrate, forming a photoresist layer over the
polysilicon layer, etching and removing portions of the polysilicon layer
beneath openings in the photoresist layer, and stripping the photoresist layer.
Thereafter, the spacers for the N-channel and P-channel devices are typically
formed by depositing a blanket layer of spacer material over the substrate, and
then applying an anisotropic etch. Arsenic and/or phosphorus are often used to
dope the source and drain for the N-channel device, and boron is often used to
dope the source and drain for the P-channel device. Since the gates for the
N-channel and P-channel devices typically have identical thicknesses, the
spacers for the N-channel and P-channel devices typically have identical sizes.

In accordance with one aspect of the invention, a method of making N-channel
and P-channel IGFETs includes providing a semiconductor substrate with a first
active region of a first conductivity type and a second active region of a
second conductivity type, forming a first gate over the first active region and
a second gate over the second active region, wherein the

second gate has a
substantially greater thickness than the first gate,
forming first spacers in
close proximity to opposing **sidewalls** of the first gate and
second spacers in
close proximity to opposing **sidewalls** of the second gate,
wherein the second
spacers have a substantially greater **width** than the first
spacers due to the
second gate having a substantially greater thickness than
the first gate, and
forming a first source and a first drain of the second
conductivity type in the
first active region and a second source and a second drain
of the first
conductivity type in the second active region.

In FIG. 1H, photoresist layer 136 is stripped, an oxide
layer with a thickness
of 30 to 150 angstroms is thermally grown on the exposed
surfaces using tube
growth at a temperature of 700 to 1000.degree. C. in an
O.sub.2 containing
ambient, and then another oxide layer with a thickness of
1000 to 1500
angstroms is conformally deposited over the structure by
plasma enhanced
chemical vapor deposition at a temperature in the range of
300 to 450.degree.
C. Thereafter, the structure is subjected to an anisotropic
reactive ion etch
that forms oxide spacers 144 adjacent to the opposing
sidewalls of gate 126 and
oxide spacers 146 adjacent to the opposing **sidewalls** of
gate 122. Spacers 144
cover portions of lightly doped source and drain regions
130 and 132, and
spacers 146 cover portions of lightly doped source and
drain regions 140 and
142. Of importance, spacers 146 are wider than spacers
144. That is, the
lateral distance that spacers 146 extend from the opposing
sidewalls of gate
122 is greater than the lateral distance that spacers 144
extend from the
opposing **sidewalls** of gate 126. For illustration purposes,
spacers 146 have a

width of about 800 angstroms, and spacers 144 have a **width**
of about 500
angstroms.

forming first spacers in close proximity to opposing
sidewalls of the first
gate and second spacers in close proximity to opposing
sidewalls of the second
gate, wherein the second spacers have a substantially
greater **width** than the
first spacers due to the second gate having a substantially
greater thickness
than the first gate; and

forming first spacers in close proximity to opposing
sidewalls of the first
gate and second spacers in close proximity to opposing
sidewalls of the second
gate, wherein the second spacers have a substantially
greater **width** than the
first spacers due to the second gate having a substantially
greater thickness
than the first gate; and

forming first spacers in close proximity to opposing
sidewalls of the first
gate and second spacers in close proximity to opposing
sidewalls of the second
gate, wherein the second spacers have a substantially
greater **width** than the
first spacers due to the second gate having a substantially
greater thickness
than the first gate; and

applying a third etch to the spacer material without using
an etch mask for the
spacer material, wherein unetched portions of the spacer
material over the
P-type active region form first spacers adjacent to
opposing **sidewalls** of the
first gate, unetched portions of the spacer material over
the N-type active
region form second spacers adjacent to opposing **sidewalls**
of the second gate,
and the second spacers have a substantially greater **width**
than the first
spacers due to the second gate having a substantially

greater thickness than
the first gate;

US-PAT-NO: 5212542

DOCUMENT-IDENTIFIER: US 5212542 A

TITLE: Semiconductor device having at least two field effect transistors and
method of manufacturing the same

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At present, complementary field effect transistors (referred to as CMOSFET
hereinafter) are employed in very large scale LSIs, for example in dynamic
random access memories, because of its characteristics of low power consumption
and easy circuit design. The N channel MOSFET and the P channel MOSFET used in
CMOS circuits have surface channel structures and buried channel structures,
respectively, as the result of being formed by simplified manufacturing
processing, as shown in FIGS. 4A and 4B.

Referring to FIG. 1B, the **width** of sidewall spacer 12 is L.sub.SW, while the
width of impurity region 10 of low concentration is L.sub.n -. L.sub.n - must
be not **less** than 0.2 .mu.m to reduce the electric field in the vicinity of the
drain which generates hot carriers. However, impurity region 10 of low
concentration cannot easily extend beneath gate electrode 4a because it is
formed by implanting ions perpendicularly, as shown in FIG. 5B. In order to
obtain L.sub.n - of not **less** than 0.2 .mu.m, impurity region 13 of high
concentration must be formed at a position far away from gate electrode 4a.
Accordingly, it is necessary to have a considerably wide L.sub.SW. A typical
value of L.sub.SW is 0.3 .mu.m.

Referring to FIGS. 7C and 7D, oxide film 11 is etched back by anisotropic
etching to form sidewall spacers 12 at the **sidewalls** of gate electrodes 4a, 4b.
The thickness of oxide film 11 is adjusted so that the **width** of sidewall spacer
12 becomes 0.15 .mu.m.

The method in accordance with another aspect of the present invention is a
method of manufacturing a complementary field effect transistor having an N
channel MOSFET including a first gate electrode and a P channel MOSFET
including a second gate electrode formed on one substrate. The first gate
electrode and the second gate electrode are formed on the semiconductor
substrate having a main surface. By implanting ions into the main surface of
the semiconductor substrate from a direction oblique to the main surface using
the first gate electrode as a mask, an impurity region of relatively low
concentration is formed extending beneath the first gate electrode in the main
surface of the semiconductor substrate at both sides of the first gate
electrode. Sidewall spacers having a **width of not less** than 0.2 .mu.m in the
direction identical to the direction of the channel length is formed on both
sidewalls of the first gate electrode and the second gate electrode. By
implanting ions using the sidewall spacers formed on the **sidewalls** of the first
gate electrode as a mask, an impurity region is formed having a concentration
higher than that of the impurity region of low concentration which joins the
impurity region of low concentration in the main surface of the semiconductor
substrate at both sides of the first gate electrode. By implanting ions using
the sidewall spacers formed on the **sidewalls** of the second gate electrode as a

mask, a P type impurity region is formed on both sides of the second gate
electrode.

There are sidewall spacers having a **width not less** than 0.2 .mu.m in the
direction identical to the direction of the channel length at the **sidewalls** of
the gate electrodes. P type impurity ions are implanted into the main surface
of the N well using sidewall spacers as a mask so the P type impurity region
will not extend below the gate electrode. As a result, a complementary field
effect transistor is obtained without the punch-through phenomenon in a P
channel MOSFET.

FIG. 1B is a sectional view of a conventional **CMOS** device comprising an N
channel MOSFET having an LDD structure.

FIG. 1C is a partial sectional view of a **CMOS** device comprising Gate/N.sup.-
overlapped LDDMOSFET.

The **sidewalls** of gate electrode 4a of N channel MOSFET 5 and gate electrode 4b
of P channel MOSFET 6 are provided with sidewall spacers 12. The **width** (LSW)
of sidewall spacer 12 in a direction identical to the direction of the channel
length is selected to be within the range of 0.2-0.3 .mu.m.

Referring to FIGS. 3C and 3D, oxide film 1 is etched back by anisotropic
etching to form sidewall spacers 12 at the **sidewalls** of gate electrodes 4a, 4b.
Oxide film 11 of the required film thickness is deposited so that the **width** of
sidewall spacer 12 in the direction identical to the direction of the channel
length is within the range of 0.2-0.3 .mu.m. Then, the N well 3 side is
covered by resist 9. By implanting N type impurity ions of relatively high
concentration into the main surface of P well 2 using gate

electrode 4a and
sidewall spacers 12 as masks, impurity region 13 having a concentration higher
than that of impurity region 10 is formed in the main surface of P well joining
impurity region 10 of low concentration. The concentration of impurity region
10 of low concentration is set to a concentration of about 1/100 of that of
impurity region 13 of high concentration for obtaining a LDD structure. Then,
resist 9 is removed.

Referring to FIGS. 3D and 3E, sidewall spacers 12 having a **width of not less**
than 0.2 .mu.m in the direction identical to the direction of the channel
length are formed on the **sidewalls** of gate electrodes 4a, 4b, followed by
implanting P.sup.+ impurity ions into the main surface of N well 3, using these
sidewall spacers as masks. This will prevent P.sup.+ impurity region 14 from
extending to beneath gate electrode 4b. Consequently, the punch-through
phenomenon shown in FIG. 8 will not occur in the P channel MOSFET.

The present invention comprises a complementary field effect transistor with
the N channel MOSFET and the P channel MOSFET formed on the same substrate, and
the method of manufacturing the same. This complementary field effect
transistor has both reliability and high speed in the N channel MOSFET, and
without punch-through in the P channel MOSFET, even though the device becomes
more minute. This gives the advantage that the scale of integration of **CMOS**
devices can be increased.

forming sidewall spacers having a **width of not less** than 0.2 .mu.m in the
direction identical to the direction of the channel length at both **sidewalls** of
said first gate electrode and said second gate electrode,